UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/624,691	07/24/2000	Nada El-Zein	JG00009	6599

22850 7590 07/11/2003

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER
BAUMEISTER, BRADLEY W

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/624,691	El-Zein et al.
Examiner	**Art Unit**
B. William Baumeister	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 28, 2003* .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *67-85, 88-100, and 102-110* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *67-85, 88-100, and 102-110* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 11
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

BWB

DETAILED ACTION

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

1. Claims 67-85, 88-100 and 102-110 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guenzer '653 in view of Kaushik et al., "Device Characteristics of Crystalline Epitaxial Oxides on Silicon;" Device Research Conference, 2000, Conference Digest 58th DRC, pp. 17-20, June 19-21, 2000 and JP 52-89070.

a. Guenzer '653 teaches a semiconductor layer 14 which may either be composed of Si or a compound semiconductor (see e.g., col. 3, lines 55-) and that is formed over a monocrystalline Si substrate 22 by means of a perovskite layer such as BTO 12 or others (col. 3, lines 45-55) and an amorphous SiOx layer 24. Guenzer does not read on those limitations of the claims that set further forth that the perovskite layer 12 and the compound semiconductor layer 14 are monocrystalline. Rather, Guenzer teaches that the epitaxial perovskite is "crystallographically oriented" which he defines to mean strongly oriented in the c-axis direction, but that the a- and b- axis directions possess a mosaic crystalline structure (e.g., col. 2, lines 5-44). Guenzer further states that the crystallographically oriented perovskite causes the resultant superposed epitaxial layer to also be a crystallographically oriented layer that does not have the very high quality of singly crystalline semiconductor material, but which is better than polycrystalline layers, so that transistors should be able to be formed therein (col. 4, lines 12-20).

To summarize, Guenzer teaches the integration of compound semiconductor layers with devices formed therein on monocrystalline Si substrates; it teaches that crystalline imperfections in the perovskite buffer will produce crystalline imperfections in this overlying epitaxial device layer; and it provides motivation as to why one would have desired to form a monocrystalline buffer and therefor a monocrystalline epitaxial device layer instead of ones that are crystallographically oriented: to produce higher quality transistors or devices.

b. Kaushik teaches the growth of monocrystalline epitaxial perovskite oxides such as STO over monocrystalline substrates which produces an amorphous SiO2 interface layer therebetween. The article does not teach the further inclusion of a compound semiconductor layer on top of the monocrystalline perovskite oxide.

c. JP '070 teaches the growth of monocrystalline (100) Si, III-Vs (such as GaAs, GaP and InP) or II-VIs (such as ZnSe and ZnTe) on monocrystalline (001) or (100) perovskite oxides such as STO, BTO, SZO and BZO.

d. It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the teachings of Kaushik and JP '070 to form a monocrystalline, epitaxial compound-semiconductor device layer on a monocrystalline Si substrate by means of a monocrystalline perovskite oxide such as STO and a layer of amorphous Si oxide for the purpose of producing an epitaxial device layer that will enable the formation of better quality components therein, as Guenzer '653 teaches is desirable.

e. Regarding the claim limitations directed towards the specific devices/circuits formed in/on the compound semiconductor and/or substrate layers (i.e.: tunnel diode and associated circuitry), Official Notice is taken that these specific devices and/or circuits as well as the associated methods of forming them were, themselves, conventional and known to those of ordinary skill in the art at the time of the invention. This assertion is evidenced by factors such as (1) various prior art references supplied in the IDS submissions in the present and/or various ones of the approximately 300 related applications; (2) the absence of any assertions in the present specification that the particular device(s) and/or circuit(s) formed on the recited semiconductor layer(s) was(/were) unknown, have any novel features beyond being integrated on the (monocrystalline Si) substrate, or produced any unexpected results; (3) Applicant's admissions/statements in the specification that III-V based tunnel diodes were known (BACKGROUND) and (4) the prior art of record that is directed towards tunnel diodes and applied in the previous rejections.

f. Further, it was well known to those of ordinary skill in the art at the time of the invention to form a wide array of active and passive devices on compound semiconductor layers instead of Si for various reasons such as (1) for producing devices and circuits that have higher frequencies and/or faster operation than is afforded by Si; and (2) because unlike Si, many conventional compound semiconductors are direct bandgap materials, enabling the formation of optoelectronic devices such as light emitters, detectors and modulators. Such conventional

compound semiconductors include many of the III-Vs (e.g, III-As, III-P, III-N and combinations thereof) and the II-VIs.

g. Moreover, it has been a decades-long-sought industry goal to be able to reliably form compound semiconductor layers on Si substrates (1) for the purpose of integrating compound semiconductor devices with Si devices on a single chip because this would reduce the number, size and/or total space of required components and reduce the length or eliminate the number of requisite, associated electrical interconnections; and (2) because the elimination of the need for a compound semiconductor wafer would greatly reduce the manufacturing costs since Si substrates are so much cheaper to produce than compound semiconductor wafers. While this desire to form compound semiconductor layers on Si substrates was conventional, the ability to actually do so has generally proven difficult because of the dissimilarities that exist between various properties of Si and the compound semiconductors, such as their dissimilar lattice constants. Conventional attempts to form compound semiconductors on Si have previously included schemes such as the use of wafer-bonding techniques and the use of intermediate buffer layers.

h. Since the prior art teaches that it was obvious at the time of the invention to have formed the compound semiconductor layer on the substrate by means of the specific buffer layer(s) as presently claimed, it would have further been obvious to one of ordinary skill in the art at the time of the invention to have formed the specifically recited components on the compound semiconductor layer and the Si layer, with the recited interconnections since the particular

devices/circuits were conventional, their was a strong and widely known motivation in the industry to integrate compound and Si semiconductor devices/circuits and because the integration of the present particular devices does not produce any unexpected results.

i. Various claims set forth that the oxide layer is formed as a monocrystalline layer and converted to an oxide layer. Under the well-established product-by process doctrine, since the claims are directed towards a structure, it is immaterial how the final amorphous structure was made since the process does not limit the structure (i.e., it is immaterial whether the amorphous layer was at one time monocrystalline).

i. Further, while the examiner assumes that Applicant intended to be referring to the perovskite layer (e.g., BSTO) layer, various claims are broad enough to read on either (1) an amorphous SiOx layer or (2) a buffer comprising of a perovskite layer and an amorphous SiOx layer, respectively. For example, claim 84--which depends from claim 73--sets forth, in part:

> "an oxide layer formed overlying the substrate...wherein the oxide layer comprises BSTO... [claim 73]
> ...wherein the oxide layer comprises and amorphous oxide layer." [claim 84]

This language is broad enough to read on a compound oxide layer comprising a BSTO layer and an amorphous SiOx layer.

ii. Similarly, claim 100--which ultimately depends from claim 83--sets forth an SiOx layer underlying the oxide layer. Claim 83, in turn, broadly sets forth an amorphous

oxide. As such, the claim reads on two amorphous SiOx layers, but since amorphous SiOx has no long-range grain boundaries, two SiOx layers is structurally equivalent to one SiOx layer.

j. Regarding claims 93 and the associated dependent claims, Applicant has asserted that these claims correspond to claim 40, which the previous examiner has indicated as being allowable. In that no reasons for the indication of allowable subject matter appear in the record, it is unclear to the present examiner why the further recitation of a GaAs buffer would be cause for allowance. Rather, the formation of tunnel diodes on GaAs is known, and the references above discuss the formation of GaAs on BSTO oxides. Moreover, the lowest portion of the GaAs layer that is formed on a perovskite (or any other material forming a heterojunction) performs the function of buffering the rest of the superposed the GaAs layer. As such, it is structurally indistinguishable whether the lowest portion of a GaAs layer that is formed on the perovskite is referred to as part of the GaAs layer or as a separate GaAs buffer. Accordingly, the indication of allowable subject matter is withdrawn.

Double Patenting

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. **The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.**

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b)

4. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application.

5. Double-patenting conflicts exist between claims of the following related issued patents and co-pending applications which includes the present application.

Serial Numbers of Related Issued Patents and Co-pending Applications:

09273929	09755691	09882063	09906138	09911445	09921905	10017596
09274268	09758723	09882064	09906730	09911446	09921910	10020898
09425945	09766046	09882067	09906769	09911447	09924481	10020900
09465623	09780119	09884082	09906782	09911448	09927393	10026446
09584601	09795784	09884149	09906783	09911455	09927396	10026812
09607207	09801881	09884150	09906784	09911456	09928356	10053588
09607236	09813779	09884981	09907703	09911457	09929018	10059409
09607237	09822499	09884982	09907704	09911458	09929019	10059411
09607239	09822499	09884983	09907705	09911459	09929020	10062429
09607386	09824259	09885409	09907707	09911460	09929021	10076450
09607408	09824273	09897059	09908695	09911464	09929022	10091452
09607420	09824376	09897128	09908707	09911465	09929024	10124460
09607434	09824388	09897965	09908860	09911466	09929261	10125410
09607722	09824615	09897968	09908883	09911469	09929748	10125486
09607744	09832354	09899996	09908885	09911472	09930145	10125540
09608807	09838273	09899997	09908886	09911473	09930170	10128262
09609071	09840213	09900882	09908887	09911475	09930171	10134506
09609262	09842734	09900883	09908888	09911478	09930175	10136324
09617640	09842735	09900885	09908891	09911484	09930176	10137369
09621130	09849159	09900887	09908892	09911487	09930188	10137383
09621771	09849172	09900921	09908897	09911488	09930243	10140939
09621779	09852109	09901109	09908898	09911490	09930247	10141876
09624296	09853744	09901110	09908902	09911491	09930254	10145734
09624526	09859700	09901601	09909905	09911492	09930259	10150065
09624690	09861636	09901905	09909906	09911493	09930260	10150066
09624691	09861637	09903740	09909936	09911494	09930261	10151950
09624698	09861638	09903741	09909937	09911495	09930270	10152783
09624699	09861639	09903742	09909938	09911496	09930275	10161743
09624754	09865428	09903743	09909939	09911496	09930276	10166196
09624803	09865429	09903784	09909940	09911507	09930278	
09624877	09865446	09904841	09909941	09911517	09930308	
09625100	09865447	09904892	09910018	09911518	09930444	
09629283	09865448	09904894	09910019	09911539	09934836	
09642558	09865449	09904895	09910020	09911542	09960402	
09656337	09866637	09905098	09910021	09911543	09975930	
09662390	09870589	09905110	09910022	09911627	09978096	
09669602	09870592	09905115	09910023	09911628	09983326	
09678372	09870828	09905116	09910024	09911629	09983854	
09689583	09870829	09905863	09910032	09911691	09983859	
09692568	09870830	09905868	09910034	09911702	09983866	
09712425	09870831	09905869	09910035	09918801	09983869	
09712875	09870832	09905902	09910044	09918802	09984471	
09721566	09870833	09905903	09910753	09919927	09985757	
09733181	09870834	09905930	09910754	09919967	09986024	
09733688	09870835	09905932	09910798	09921894	09986034	
09740219	09870836	09905933	09910799	09921895	09986534	
09740268	09870837	09905934	09911412	09921896	09986899	
09753808	09871958	09905935	09911420	09921898	09993514	
09755340	09874984	09905980	09911429	09921900	09993523	
09755341	09882062	09905981	09911444	09921901	09994066	

6. While it is true that the Examiner has the burden to show how a rejection is specifically applied to each claim, the exemplary showing with respect to the claims individually discussed below establishes a *prima facie* showing of the unpatentability of the instant claims and is sufficient to give the applicant fair notice of how the rejection is applied to each and every other claim. Further, an analysis of all of the claims in the approximately 330 related applications would be an extreme burden on the Office requiring millions of claim comparisons. Accordingly, the Office is shifting the burden to the applicants to show, if they can, patentable distinctions between the instant claims and those of the other applications and patents. Specifically, in order to resolve the conflict between applications, applicant is required to:

(1) file terminal disclaimers in each of the related, applications terminally disclaiming each of the other approximately 330 applications;

(2) provide a statement attesting to the fact that all claims in the approximately 330 applications have been reviewed by applicant and that no conflicting claims exists between the applications. Applicant should provide all relevant factual information including the specific steps taken to insure that no conflicting claims exist between the applications; or;

(3) resolve all conflicts between the claims in the above identified approximately 330 applications by identifying how all the claims in the instant application are distinct and separate inventions from all of the claims in all of the other approximately 330 identified applications. Note: the examples provided below are merely illustrative of the overall

problem. Only addressing/correcting the specifically identified conflicts would **not** satisfy the requirement.

Further, due Applicant's better familiarity with the related applications, Applicant now has the burden of confirming that the preceding list is accurate and complete, or must take appropriate action(s) to assure that no such conflicts exist in any other applications that have been inadvertently omitted from the preceding list, but do in fact possess related subject matter.

Applicant is reminded that obviousness-type double patenting analysis entails a two-step process: (1) the claims of this application and the other approximately 330 applications must be construed; and (2) the claims of this application must be compared with the claims of the other applications to determine whether the differences in subject matter between the two claims render the claims patentably distinct. See Georgia-Pacific Corp. v. United States Gypsum Co., 195 F.3d 1322, 1326, 52 USPQ2d 1590, 1593 (Fed. Cir. 1999), and General Foods Corp. v. Studiengesellschaft Kohle, 972 F.2d 1272, 1279, 23 USPQ2d 1839, 1844 (Fed. Cir. 1992). As the Court of Customs and Patent Appeals (CCPA) explained: "[t]he fundamental reason for the rule [against "double patenting"] is *to prevent unjustified timewise extension of the right to exclude* granted by a patent no matter how the extension is brought about." In re Van Ornum, 686 F.2d 937, 943-44, 214 USPQ 761, 766 (CCPA 1982) (brackets and emphasis in the original) (quoting In re Schneller, 397 F.2d 350, 354, 158 USPQ 210, 214 (CCPA 1968)).

Failure to comply with the above requirement will result in abandonment of the application. However, the requirement will be held in abeyance until allowable subject matter has been indicated by the examiner.

7. The following claim comparisons are examples of conflicts between three of the copending applications:

S.N. 09/908,892; claims 11

A process for fabricating a semiconductor structure comprising:

providing a monocrystalline silicon substrate;

depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;

forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate;

epitaxially forming a layer of intermetallic compound overlaying the monocrystalline perovskite oxide film; and

epitaxially forming a monocrystalline compound semiconductor layer overlying the layer of intermetallic compound.

S.N. 09/755,340; claims 17, 19 and 20:

[Claim 17] A process for fabricating a semiconductor structure comprising the steps of:

providing a monocrystalline substrate;

epitaxially growing [an] accommodating buffer layer overlying the monocrystalline substrate;

forming an amorphous layer on the monocrystalline substrate during the growth of the accommodating buffer layer; and

forming a monocrystalline conductive layer over the accommodating buffer layer;

[Claim 19] epitaxially growing an additional monocrystalline layer above the monocrystalline conductive layer;

[Claim 20] wherein the step of [claim 19] includes growing a semiconductor material layer.

S.N. 09/986,024; claim 169:
A process for fabricating a semiconductor structure comprising:
providing a monocrystalline silicon substrate;
depositing a monocrystalline perovskite oxide film overlying the monocrystalline silicon substrate, the film having a thickness less than a thickness of the material that would result in strain-induced defects;
forming an amorphous oxide interface layer containing at least silicon and oxygen at an interface between the monocrystalline perovskite oxide film and the monocrystalline silicon substrate; and
epitaxially forming a monocrystalline compound semiconductor layer overlying the monocrystalline perovskite oxide film.

8. A comparison of the claims shows that all three applications set forth the method steps of providing a monocrystalline substrate; an accommodating buffer (or perovskite) layer; an amorphous oxide interface therebetween; and at least a monocrystalline semiconductor layer over the buffer/perovskite. The respective sets of claims are not identical because:

a. Claims 17, 19 and 20 of the '340 application are broader than claim 11 of the '892 application because the '340 claims do not further require that the monocrystalline substrate be Si; that the amorphous oxide interface layer also contain silicon; that the accommodating buffer specifically be a monocrystalline perovskite; that the conductive layer specifically be an intermetallic compound; nor that the monocrystalline semiconductor layer be a compound monocrystalline semiconductor layer.

b. Claim 169 of the '024 application is broader than claim 11 of the '892 application because the '024 claim does not require the additional presence of the epitaxially grown intermetallic compound layer.

9. Accordingly, claims 17, 19 and 20 of the '340 application are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of the copending '892 application. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 11 of the '892 application anticipates claims 17, 19 and 20 of the '340 application as explained above. See e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985) for the proposition that an obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but an examined application claim is not patentably distinct from the reference claim(s) because the examined claim is either anticipated by, or would have been obvious over, the reference claim(s). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

10. Similarly, claim 169 of the '024 application is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 11 of the copending '892 application. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 11 of the '892 application anticipates claim 169 of the '024 application as explained above. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

11. While not specifically addressed herein, similar double-patenting conflicts also exist between the product claims of various applications as well. Moreover, while the Office has a long established policy of generally requiring restrictions between semiconductor product claims (class 257) and method claims (class 438) in a given application, this policy does not negate Applicant's responsibility for ensuring that no conflicts exist between those applications presenting product claims and those applications presenting method claims. This is because it is also well established agency policy that restricted product and method claims may be subject to rejoinder during the course of prosecution. See MPEP 821.04.

Response to Arguments

12. Applicant's arguments filed 4/28/03 have been fully considered but they are not persuasive.

a. Applicant argues that the Examiner's taking of Official Notice is deficient because it is so general, and so non-specific, that it effectively prevents Applicants from rebutting the present rejection, which relies upon the Official Notice to supply particular claim limitations. To support this position Applicant asserts (REMARKS):

> [b]ecause for a proper *prima facie* case of obviousness to be presented the prior art must be considered as a whole, and motivation must exist for the proper combination of elements therein, it is essentially impossible for applicants to discuss whether and how the rejection might or might not meet these requirements. Applicants are entitled to evidence on the issue of Official Notice, and further are entitled to the Examiner's reasoning with regard to specific limitations in the pending claims. For example, how is Applicant to respond to the rejection of [particular claim(s)] when the only information provided in the Official Action regarding the claimed [components] is a non-specific and unsupported assertion that such components were known, perhaps in other contexts, in different arrangements and different devices? The reasoning is simply too vague. In fact, the reasoning is so vague, and so lacking in specifics, that it fails to present a *prima facie* case of obviousness supportable by reference to objective evidence. In this regard, Applicants again note their seasonable challenge to the taking of Official Notice, and require supplementation of the record along with a reasoned statement of rejection, or a Notice of Allowance.

b. First, the Examiner notes that the prior rejection did set forth support for all of the layers, elements, components and/or interconnections that were claimed. For example, the specific order and compositions of the respective recited layers were taught by the various references specifically cited in the rejection. Further, the Examiner explained that the specific devices, components and interconnections that were formed on/in/between the various layers

were conventional, and specifically provided a basis for this conclusion: either (1) by supplying references that taught these particular components; (2) by citing to prior-art references in Applicant's IDS submission(s) that disclose these components; and/or by citing specific portions of Applicant's specification which acknowledges that these particular components were conventional. The Office Action further provided motivation as to why these various references and prior-art admissions were combined in the manner set forth in the rejection. As such, the rejection does, in fact, set forth a *prima facie* case of obviousness with sufficient support and specificity of reasoning such that Applicant can properly address the rejection.

c. In further regard to the argument that the taking of Official Notice was unsupported and too vague, the Examiner notes that the bases were sufficiently supported and evidenced because the Examiner pointed to various sources that provide support for the conclusion that the particular devices were conventional. For example, in many instances the Examiner pointed out portions of the specification where Applicant acknowledged that the devices were "typical." As such, the Examiner has already provided evidence sufficient to support Official Notice, and the burden has shifted to Applicants to rebut or refute this showing, for example by (1) providing sufficient evidence that these statements in the specification were not admissions that the "typical devices" constitute prior art (e.g., that the device was only known in-house) or (2) specifically pointing out those particular claim limitations that further distinguish the device/component *as claimed* from the "typical" or conventional device/component. Applicant has not made any such arguments.

Further, the fact that the rejection's reliance was upon propositions (e.g., that the particular devices/components were known) that were general, does not indicate that the rejections were overly broad or vague. Rather, it is indicative of the breadth of the claims as currently presented: i.e. that the rejection of the claim(s) did not require a showing that was any more specific than that which was made because the claim language was so broad.

d. Accordingly, because the rejection sufficiently explained the Examiner's position as to why all of the devices and layers were known, why one skilled would have wanted to combine all of the layers and specific components in the manner set forth, and because sufficient evidence has already been provided to support those portions of the rejection that rely upon Official Notice, the rejections are still deemed to be proper.

Allowable Subject Matter

13. The following is a statement of reasons for the indication of allowable subject matter:

a. The Examiner notes that the common feature of all of the bulk-filing status applications relates to the buffer structure. Specifically, most of the applications set forth the following layers with the optional inclusion of further layers and/or devices: monocrystalline Si substrate / amorphous SiOx interface layer / monocrystalline perovskite (such as BaSrTiO3 or BSTO) accommodating buffer / monocrystalline compound semiconductor. Some applications--such as those directed towards waveguide structures--form other monocrystalline perovskites or oxides over the accommodating BSTO layer instead of a compound semiconductor layer.

b. The Examiners assigned to the bulk-filing project have found only two references which teach forming a mono-perovskite on mono-Si by means of an amorphous SiOx interface layer: Kaushik (already made of record in the last Office Action) and Eisenbeiser et al., Field effect transistors with SrTiOs gate dielectric on Si," 6 March 2000, Applied Physics Letters, Vol. 76, No. 10, pp.1324-1326 (which appears to contain substantially similar subject matter and which is included herewith). Both of these articles include authors who are or were employed by Motorola, and more specifically include authors Dr. Ravi Droopad and Dr. Jamal Ramdani. Further, various additional news releases/publications quote either Dr. Droopad, Dr. Ramdani and/or Motorola spokespersons as asserting that (1) Dr. Droopad invented the mono-Si/amorphous SiOx/STO structure (for use as a FET gate dielectric); (2) Dr. Ramdani came up with the idea of employing this particular structure as a buffer system for growing monocrystalline compound semiconductor layers on Si substrates; and (3) that Motorola has filed more than 270 patent applications based on this technique or concept. *See, e.g.*, Weiss, "Speed demon gets hooked on silicon," Science News Online, 9/15/2001; "Motorola develops new super-fast chip," USA Today, 9/4/2001; Valigra, "Motorola Lays GaAs on Si Wafer," AsiaBiz Tech, Nov. 2001; and "Holy Grail! Motorola claims high-yield GaAs breakthrough," Micromagazine.com (no date available).

c. The record is presently unclear as to (1) the exact participation others may have had in inventing this subject matter; and (2) whether Dr. Droopad and Dr. Ramdani were employed by Motorola at the time of the respective inventions.

d. The Examiner further notes that various ones of the present applications do not list one or both of Dr. Droopad and Dr. Ramdani as an inventor. Also, various applications--irrespective of inventorship--were filed more than one year after the publication of the Eisenbeiser and/or Kaushik references.

e. The Kaushik and Eisenbeiser references would not be available as prior art if Applicants (1) provide proper and sufficient affidavit evidence of who were the actual inventor(s) of the mono-Si/amorphous SiOx/STO structure; (2) properly petition to correct the inventorship of any applications not including this (/these) inventor(s); and/or (3) properly petition and amend the status of those applications filed more than a year after the publication of the Eisenbeiser reference so as to make those applications continuations or continuations-in-part of application #09/502,023, now US Patent # 6,492,257, which was filed on February 10, 2000 and issued on May 21, 2002, and of which Drs. Ramdani and Droopad were named inventors. (See MPEP 201.11.V for the Office requirements regarding the untimely filing of Priority Benefit Claims and whether this option is available to the applicants in the present circumstances.)

f. If Applicant takes the necessary steps to properly remove the Kaushik and Eisenbeiser references as available prior art, and is thereby successful in overcoming all 35 USC 102(a), (b), (e), (f) and 103(a) issues based upon any of these section 102 paragraphs, the claims would be allowable if they include sufficiently specific limitations relating to these particular layers

and their interrelationships. For example, the claims would be allowable if Applicants properly include at least the following limitations:[1]

a monocrystalline silicon substrate;

an amorphous silicon oxide layer formed directly on the silicon substrate;

a monocrystalline $Ba_xSr_{1-x}TiO_3$ layer formed directly on the amorphous silicon oxide layer, wherein ($0 \leq x \leq 1$); and

a monocrystalline [compound semiconductor][2] layer formed on the $Ba_xSr_{1-x}TiO_3$ layer.

g. If such amendments are made, any restricted claims previously withdrawn from consideration for being directed towards a non-elected invention (such as in response to a product/method, subcombination-usable-together or a combination/subcombination restriction) that depend from such a claim or otherwise include all such claim language, would be subject to rejoinder in accordance with the rejoinder guidelines of MPEP, Chapter 800.

h. The Examiner further notes that a search of the prior art failed to disclose or reasonably suggest a buffering-layer system wherein the BSTO accommodating buffer is subsequently converted to an amorphous layer. As such, any claims directed towards this

---

[1]Applicant is invited to contact the Examiner with any questions regarding specific proposals for substantively broader or alternative claim language.

[2]As noted hereinabove, some applications set forth layers other than compound semiconductors formed on the BSTO so this term would need to be amended accordingly.

embodiment would be allowable if they include at least the following limitations--*irrespective of whether the Kaushik and Eisenbeiser references are available as prior art*:

a monocrystalline silicon substrate;

an amorphous $Ba_xSr_{1-x}TiO_3$ layer formed on the silicon substrate, wherein ($0 \leq x \leq 1$);

and

a monocrystalline [compound semiconductor][3] layer formed on the $Ba_xSr_{1-x}TiO_3$ layer.

i. It is further noted that some applications currently possess product claims that recite, *inter alia*, "a monocrystalline $Ba_xSr_{1-x}TiO_3$ layer," and also include further claims depending therefrom that recite language to the effect of: wherein the monocrystalline BSTO layer is subsequently heat-treated to convert it to an amorphous layer. **Such claim language is objectionable under 35 USC 112, 4th paragraph** because such depending claims do not further limit nor add additional limitations to the previously claimed subject matter. Rather, such claim language modifies the structure of the parent claim. Accordingly, Applicant should review all of the claims and correct any such dependencies by canceling the claim or placing it independent form.

---

[3]See the previous footnote.

14. If (1) all of these actions cited above are properly undertaken as required, (2) terminal disclaimers are properly filed, and (3) no other significant issues remain, the Examiner will *consider* entry of amendments that place all of the claims in condition for allowance, even if submitted after prosecution is closed.

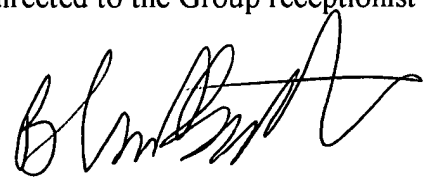
Conclusion

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister,** at **(703) 306-9165.** The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Eddie Lee, can be reached at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.



B. William Baumeister

Primary Patent Examiner, Art Unit 2815

July 5, 2003